

REMARKS

Claim Rejections - 35 U.S.C. §103

Claims 1, 2, 4, 5, 7, 8, 10, 11, 12, 14, 15, 17, 18

It is Applicant's understanding that the invention specified in Claims 1, 2, 4, 5, 7, 8, 10, 11, 12, 14, 15, 17, 18 are not anticipated by Papathomas.

In claims 1, 2, 4, 7, 8 10, 11, 12, 14, 15, 17, and 18 Applicant claims "an electronic device or system comprising a substrate having at least one build up layer, a semiconductor die, and at least one interconnect disposed between the substrate and the semiconductor die." The substrate is bonded with the semiconductor die by the at least one interconnect, wherein the at least one build up layer comprises at least one binder and at least one filler; and the at least one filler has a negative coefficient of thermal expansion. That is, Applicant claims an electronic device comprising a "substrate featuring a build up layer embedded within, wherein the build up layer comprises a binder and a filler having a negative coefficient of thermal expansion."

Applicant's claim of an electronic device comprising a substrate featuring a build up layer embedded within, which comprises a binder and a filler having a negative coefficient of thermal expansion, is supported in the application. Figure 1

of the application illustrates substrate 100 featuring build up dielectric material 120 within. That is, build up dielectric material 120 is part of substrate 100, wherein substrate 100 is subsequently bonded to a semiconductor die.

It is the Applicant's understanding that Papathomas fails to disclose an electronic device comprising a substrate featuring a build up layer embedded within, which comprises a binder and a filler having a negative coefficient of thermal expansion. Papathomas discloses an electronic package 10 which includes a substrate 2 having an upper surface 4, a semiconductor chip 6 mounted on a portion of the upper surface of the substrate and electrically coupled to the substrate 2. The semiconductor chip having a bottom surface 8 and at least one edge surface 12 being substantially perpendicular to the bottom surface and a material, wherein the material has an encapsulant composition which includes a filler material. It is Applicant's understanding that the material comprising the encapsulant composition is between the substrate and the semiconductor chip and along with substrate 2 are separate and individual components of the electronic package.

Therefore, it is Applicant's position that Papathomas does not teach an electronic device comprising a substrate featuring a build up layer embedded within, wherein the build up layer comprises a binder and a filler having a negative coefficient of thermal expansion. Also, the Applicant requests claims 2-3, 5-6, 8-9, 18-19 are allowable upon the allowance of base claims 1, 4, 7, and 17.

The Examiner has objected to Claim 13 but has indicated that it would be allowable if rewritten in independent form including all intervening claims.

Applicant has amended **base claim 10** to include the limitations of dependent claim 13 and intervening claim 11. Applicant has cancelled claims 11 and 13. Also, claim 12 has been amended to be dependent upon amended claim 10. Accordingly, claim 10 is now in condition for allowance.

Also, the Examiner has objected to Claim 16, but has also indicated that it would be allowable if rewritten in independent form including all intervening claims. Applicant has amended **base claim 14** to include the limitations of dependent claim 16 and intervening claim 15. Applicant has cancelled claims 15 and 16. Accordingly claim 14 is now in condition for allowance.

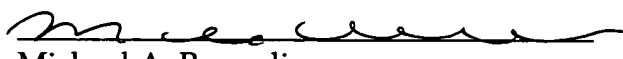
Additionally, the Examiner has allowed Claim 20 which the Applicant accepts and respectfully leaves Claim 20 un-amended.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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